BY FAX -- 6 Pages

XA-10084
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

First Named Inventor: SAKAMOTO, KAZUO Art Unit: 2116

Appln. No.: 10/827,288 Examiner: Rahman

Filed: April 20, 2004 Conf. No.: 2625

For: DATA PROCESSING DEVICE AND MOBILE DEVICE

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PROPOSAL FOR EXAMINER'S AMENDMENT

Dear Examiner Rahman:

Per your request, please see the accompanying proposed amendments to the specification.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000
MWS/dmt

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AMENDMENTS TO THE SPECIFICATION:

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Please substitute the following paragraph for the paragraph beginning at line 2.

The memory card interface unit ~~221~~ of FIG. 7 is constituted by: a flip-flop 251 for frequency division which is caused to perform a latch operation by a system clock Φs and generate a synchronous clock CLK for data transfer to the memory card 100 having a period double the period of the system clock Φs; an output buffer 252 for outputting, from an external terminal 241, a clock signal outputted from the flip-flop 251 to the outside of the chip; an I/O control logic circuit & level shift circuit 253 for determining an input/output state based on an I/O control signal Sio supplied from an I/O register ~~223~~ or the like and controlling the output buffer 252 and the like; an input logic gate 254 and an input latch 255 each for latching a data signal inputted to the external terminal 242 from the outside of the chip; and the like. The memory card interface unit ~~221~~ is constructed to return the clock signal at the point B outputted from the output buffer 252 to the input latch 255 via an OR gate ~~G3~~ or the like and latch the data signal inputted to the external terminal 242 at that

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time in synchronization with a return clock CLK' such that the latched data signal is supplied to each of internal circuits.

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Please substitute the following paragraph for the paragraph beginning at line 3.

In the specifications of the MMC card, it is defined that data is outputted on the falling edge or rising edge of the input clock CLK, i.e., with a timing after a lapse of (Tc - 5ns) from the timing t1 of FIG. 8B or with a timing after a lapse of (Tc - 5ns) from the timing t2 of FIG. 8B, where Tc is the period of clock signal at point A. Thus, in the MMC card, data is outputted in synchronization with the falling edge or rising edge of the clock (MMCA Technical Committee "The Multi Media Card System Specification Version 3.1") as shown in FIGS. 8D and 8E. As shown in FIGS. 8D and 8E, the data at point E is delayed by T3 relative to the data at point D.

Please substitute the following paragraph for the paragraph beginning at line 12.

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Therefore, the specifications of the interface with the MMC card of the present LSI have been designed to guarantee, for the timing of the data signal outputted from the MMC card, a 5-ns set-up time Ts and a 5-ns hold time Th around the timing t3 delayed by the time T2, shown in FIG. 8C, from the rising edge t2 of the clock CLK at point B, which is delayed by T1 relative to the clock at point A.

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Please substitute the following paragraph for the paragraph beginning at line 17.

FIGS. 3A-3F are ~~is~~ a timing chart showing timings (data output on the falling edge of a clock) of signal transmission and reception to and from an MMC card in the memory card interface unit of FIG. 2;

Please substitute the following paragraph for the paragraph beginning at line 21.

FIGS. 4A-4F are ~~is~~ a timing chart showing timings (data output on the rising edge of the clock) of signal transmission and reception to and from the MMC card in the memory card interface unit of FIG. 2;

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Please substitute the following paragraph for the paragraph beginning at line 10.

FIGS. 8A-8G are ~~is~~ a timing chart showing timings of signal transmission and reception to and from an SD card and an MMC card in the memory card interface of FIG. 7 examined prior to the present invention.

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Please substitute the following paragraph for the paragraph beginning at line 22.

This allows the clock varying with a timing delayed by T2 from the rising edge of the signal at the point B as the external terminal 241 defined in the specifications of the MMC card to be supplied to the input latch 255, satisfies the set-up time Ts and the hold time Th, and prevents the occurrence of a set-up violation and a hold violation. Data output at point D and point E are shown in FIGS. 3E and 3F.

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Please substitute the following paragraph for the paragraph beginning at line 3.

In the MMC card, the outputting of data is performed in synchronization with any of the falling and rising edges of the clock. FIG. 4 shows timings for outputting (output on the rising edge of the clock) the data signal from the MMC card and inputting the data signal to the microcomputer, shown in FIGS. 4E and 4F. If the transmission line is ideal, the signal at the point B as the external terminal 241 for outputting the clock has a waveform delayed by T1 from the clock at the point A as indicated by the broken line of FIG. 4C. However, even when the waveform of the signal at the point B has been assumedly deformed as indicated by the solid line under the influence of a reflected wave resulting from an impedance mismatch or the like, the input latch 255 latches data on the rising edge of the clock CLK' of FIG. 4D which is obtained by delaying the clock at the point B', which is delayed by T1' shown in FIG. 4B, by the time T2' corresponding to the magnitude of the load in the variable delay circuit 257 so that a set-up violation and a hold violation will not occur.

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